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- Patent Application -

A Lateral Thyristor Structure for Protection Against Electrostatic Discharge

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Description

A Lateral Thyristor Structure for Protection Against Electrostatic Discharge

The invention relates to a lateral thyristor structure for protection against electrostatic discharge.

As Figure 1 shows, integrated circuits have at least one interior circuit 4 which requires protection, two supply terminals 1, 2, and one terminal 3 for input or output. In the event of an electrostatic discharge (ESD) in the input/output, a very high voltage/a very strong current can reach the functional elements of the interior circuit 4. E.g. gate oxides or the diffusions of output transistors are affected by this.

Furthermore, the discharge can also reach the supply lines (1, 2) through bipolar parasitic elements, which are always present. In both cases, irreversible damage can be done to the integrated circuit. Consequently, clamping devices 5 are usually attached to the supply connections 1, 2, to protect the supply lines and the elements associated therewith. Integrated circuits sometimes have a certain self-protection through inherent parasitic bipolar elements, but generally this is not sufficient.

Especially in the case of circuits which operate with high supply voltages (e.g. 8 V), and which therefore have special high-voltage transistors with a drift zone, the inherent parasitic elements trigger too late or not at all. Self-protection therefore practically does not exist and the input/output 3 can be damaged by ESD.

For this reason - as shown e.g. in the German initial Patent Disclosure DE 41 35 522 - a clamping circuit 6 is added to the input/output for clamping against a supply line 2. In the event of an electrostatic discharge (ESD), this reduces the voltage at the input/output to a tolerable value and arrests the discharge. As a rule, a clamping circuit also protects the other supply connection 1, for example by means of a diode 7. For most input/output circuits, only a parallel protector is feasible, since, as a rule, a series resistor must not be inserted. Thyristors, field oxide transistors, or diodes are used as protection elements.

A problem with diodes is that the voltage at the diode can become quite large in the case of high currents, especially in the non-conducting direction. As a result, sensitive gate oxides and diffusions in the interior circuit that is being protected can become damaged. Furthermore, diodes are very cumbersome due to their large area, especially in the case of integrated circuits with several inputs and/or outputs.

Field oxide transistors can indeed clamp the voltage relatively well. However, depending on the external or internal circuitry of the input/output, it can happen that the field oxide transistor in the application circuit, after firing, remains in a very low-ohm state with average voltage, thus interfering with the function of the input/output. For example, if an external source can deliver sufficient current at high voltage, it can happen that a transient at the input/output triggers the clamping element and, due to the "soft firing characteristic" of the field oxide transistor structure, it is no longer quenched. But this disturbs the function of the circuit to such an extent that only turning it off and then turning it on again quenches the field oxide transistor structure and thus reestablishes the original functionality of the circuit.

Transistors without any special firing arrangement, draw so much current in their switched-on state ("hard firing characteristic"), that the external-internal source is strongly loaded and the thyristor in any case quenches, due to the voltage collapse of the source. However, the protective effect is limited by a relatively high firing voltage, so that it is perfectly possible for the circuit to be damaged before the firing voltage is reached.

Finally, a special high-voltage thyristor with a high-voltage transistor as the firing element does indeed also clamp the voltage to levels low enough that no sensible external/internal circuitry can cause a "stuck condition." However, a high-voltage transistor as firing element fires so late, due to the drift zone, that sensitive structures can already be damaged.

It is therefore the object of the present invention to specify a thyristor structure to protect against electrostatic discharge, which has a lower firing voltage and which furthermore cannot remain stuck in its switched-on state.

This object is achieved by a thyristor structure in accordance with Claim 1. Modifications and developments of the inventive idea are the subject of the subclaims.
The advantage of the invention is that the conflict between firing behavior on the one hand and switch-off behavior on the other hand is eliminated with little expense. The invention accomplishes this by combining a field oxide transistor, with its good switch-on behavior, with a thyristor, with its good switch-off behavior.

In detail, this is achieved especially by a lateral thyristor structure for protection against electrostatic discharge, cotaining a semiconductor substrate of a first conduction type, with a surface and a well region of a second conduction type, opposite to the first one, which is introduced into the surface of the semiconductor substrate. Further a first, strongly doped region of a second conduction type is introduced into the surface of the semiconductor substrate , and is electrically connected to a first terminal. A second, strongly doped region of a first conduction type is introduced into the well region and is electrically connected to a second terminal. A third, strongly doped region of another, second conduction type is introduced into the well region, and is electrically connected to the second terminal, and is spatially situated between the first, strongly doped region and the second, strongly doped region. Finally, a fourth, strongly doped region of the second conduction type is introduced into the surface of the semiconductor substrate and into the well region, and is spatially situated above the pn junction that is formed between the semiconductor substrate and the well region, and between the third, strongly doped region and the first, strongly doped region.

Since the inventive lateral thyristor structure for protection against electrostatic discharge has a firing voltage of approximately 12 volts, it achieves effective protection even for VLSI circuits in CMOS technology, whose transistors have very thin gate oxides and short channel lengths.

This low ignition voltage of approximately 12 volts is achieved in that the electric field between the semiconductor substrate and the fourth, strongly doped region of the second conduction type, which is introduced into the surface of the semiconductor substrate and into the well region is higher than the electric field between the well region and the semiconductor substrate. This results in an avalanche breakdown between the semiconductor substrate and the fourth, strongly doped region, which is introduced into the surface of the semiconductor substrate and into the well region. The charge carriers generated by the avalanche breakdown then make the base of an npn transistor conducting, this npn transistor being composed of the first, strongly doped region of the second conduction type, the semiconductor substrate, and the well region. The well region forms the collector of the npn transistor; the semiconductor substrate forms its base; and the first, strongly doped region forms its emitter. Because the base is made conducting by the charge carriers generated from the avalanche breakdown, the npn transistor is switched on, so that current flows from the anode to the cathode in the lateral thyristor structure.

The inventive, lateral thyristor structure for protection against electrostatic discharge can be incorporated without any problem into currently available CMOS processes. This means that, without great modification, especially without further masks and special steps, the lateral thyristor structure can be integrated monolithically into a CMOS-IC. However, it is also conceivable that the lateral thyristor structure is integrated into other semiconductor circuits, which are derived from other processes. In this connection, one can think of biCMOS processes, various processes of power semiconductors, and various DRAM processes.

Accordingly, field oxide regions, such as are customary in CMOS techniques, preferably are situated between the first, strongly doped region and the fourth, strongly doped region, also between the second, strongly doped region and the

fourth, strongly doped region. These field oxide regions are generated in CMOS technologies by the thermal oxidation of silicon. For this purpose, the semiconductor substrate is placed into a furnace at about 1000EC, and its surface is exposed to a stream of pure oxygen or of inert nitrogen with a portion of water vapor. In a further development of the present invention, several, preferably two, lateral thyristor structures can be integrated into the semiconductor substrate next to one another, preferably surrounded by a substrate contact ring. The second, strongly doped regions of the first conduction type, which are introduced into the well region, preferably are placed outward, so that the semiconductor substrate is maintained at a defined potential all around the lateral thyristor structures. This achieves effective "latch-up" protection. This means that the environment of the lateral thyristor structures is protected against unintended firing.

Furthermore, the thyristors are coupled better to one another in this way, which prevents one-sided turn-off. This makes the turn-off problem much less severe, and thus the current which the structure requires in the turned-on state always remains a maximum.

A further development consists in exchanging regions 23 and 24, which results in a different firing behavior (later) and turn-off behavior (more current is required).

It is also possible to introduce into a field oxide region a region of the second conduction type, equipped with a terminal, the terminal being connected to the circuit that is being protected.
The invention will be explained in more detail below, in terms of the embodiments shown in the figures.

Figure 1 shows a circuit arrangement for protection against electrostatic discharge.

Figure 2 shows a section through a lateral thyristor structure for protection against electrostatic discharge, in accordance with the prior art.

Figure 3 shows a section through an unsymmetric lateral thyristor structure for protection against electrostatic discharge, in accordance with the present invention.

Figure 4 shows a section through a symmetric lateral thyristor structure for protection against electrostatic discharge, in accordance with the present invention.

Figure 5 shows a section through an unsymmetric lateral thyristor structure, as an alternative to Figure 3, for protection against electrostatic discharge in accordance with the present invention.

Figure 6 shows an application of the thyristor structure of Figure 5, in connection with the circuit arrangement, of Figure 1, for protection against electrostatic discharge.

Figure 7 shows a section through an unsymmetric lateral thyristor structure, as another alternative to Figure 3, for protection against electrostatic discharge, in accordance with the present invention.

Figure 2 schematically shows a section through a lateral thyristor structure for protection against electrostatic discharge, such as is known, for example from R.N. Rountree et al. "A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes," 1988, EOS/ESD Symposium Proceedings, pages 201-205.

The lateral thyristor structure is integrated into a semiconductor substrate 10. The semiconductor substrate 10 is weakly p-doped. The weakly p-doped semiconductor substrate 10 is electrically connected to a cathode 16, via the substrate contact 19, a strongly p-doped region. A well region 11, which is weakly n-doped, is diffused into the weakly p-doped semiconductor substrate 10.

A first, strongly n-doped region 12 is diffused into the surface of the weakly p-doped semiconductor substrate 10. This n-doped region is likewise connected to the cathode 16.

A strongly p-doped region 13 and a strongly n-doped region 14 are diffused into the surface of the weakly n-doped well region 11. The strongly p-doped region 13 and the strongly n-doped region 14 are both electrically connected to an anode 17.

In the prior art shown here, the strongly p-doped region 13 and the strongly n-doped region 14 directly adjoin one another. However, it is also possible that the strongly p-doped region 13 and the strongly n-doped region 14 are spatially separated from one another, for example by a field oxide region (not shown). A field oxide region 15 is situated between the first strongly n-doped region 12 and the strongly p-doped region 13. The field oxide region 15 is situated spatially above the pn junction which is formed between the weakly n-doped well region 11 and the weakly p-doped semiconductor substrate 10. Finally, the lateral thyristor structure is spatially separated from other semiconductor structures, which are not shown here, which are introduced into the semiconductor substrate 10, and which form the circuit that is being protected.

The strongly n-doped region 12 forms the emitter of a pnp transistor. The weakly p-doped semiconductor substrate 10 forms the base of this npn transistor. The weakly n-doped well region 11 finally forms the collector of an npn transistor. The weakly p-doped semiconductor substrate 10 furthermore forms the collector of a pnp transistor. The weakly n-doped well region again forms the base for this pnp transistor. Finally, the strongly p-doped region 13 forms the emitter of this pnp transistor.

When the voltage between the anode 17 and the cathode 16 is less than about 50 volts, the pn junction between the weakly n-doped well region 11 and the weakly p-doped semiconductor substrate 10 is nonconducting, so that the lateral thyristor structure conducts only a very small current. However, if the voltage between the anode 17 and the cathode 16 exceeds approximately 50 volts, an avalanche breakdown occurs, so that charge carriers are generated at the pn junction between the weakly n-doped well region 11 and the weakly p-doped semiconductor substrate 10.

This avalanche breakdown generates charge carriers at the base-collector junctions of the two bipolar transistors, namely the npn transistor and the pnp transistor, so that the lateral thyristor fires.

Figure 3 shows a lateral thyristor structure for protection against electrostatic discharge, in accordance with the present invention. The lateral thyristor structure is introduced into the surface of a weakly p-doped semiconductor substrate. The weakly p-doped semiconductor substrate 20 is electrically connected to the cathode 26 via the substrate contact ring 31, a strongly p-doped region. A weakly n-doped well region 21 is diffused into the surface of the weakly p-doped semiconductor substrate 20. Furthermore, a strongly n-doped region 22 is diffused into the surface of the weakly p-doped semiconductor substrate 20, and is likewise electrically connected to the cathode 26. Further, a strongly p-doped region 23 and a strongly n-doped region 24 are diffused into the weakly n-doped well region 21, and both are electrically connected to the anode 27.

The strongly p-doped region 23 and the strongly n-doped region 24 are situated in the weakly n-doped well region 21 and directly adjoin one another. However, it is also conceivable that the strongly p-doped region 23 and the strongly n-doped region 24 in the weakly n-doped well region 21 are spatially separated, for example by a field oxide region (not shown).

Furthermore, the weakly p-doped semiconductor substrate 20 has a field oxide region 28, which is situated between the strongly n-doped region 22 and a strongly n-doped region 25. The strongly n-doped region 25 is introduced into the surface of the semiconductor substrate 20 and into the well region 21. It is spatially arranged above the pn junction that is formed between the weakly p-doped semiconductor substrate 20 and the weakly n-doped well region 21. The strongly n-doped region 25 can here be diffused in or can be introduced by means of ion implantation.

Another field oxide region 29 is situated in the surface of the strongly n-doped well region, between the strongly n-doped region 25 and the strongly p-doped region 23. The entire lateral thyristor structure finally is bounded by the field

oxide regions 30, which spatially separate the lateral thyristor structure from other circuit components that are integrated into the semiconductor substrate 20.

The strongly n-doped region 22 forms the emitter of an npn transistor; the weakly p-doped semiconductor substrate 20 forms the base of this transistor; the weakly n-doped well region 21 forms the collector of this npn transistor. Further, a pnp transistor is also present in the lateral thyristor structure shown in Figure 3. The base of this pnp transistor is formed by the weakly n-doped well region 21. The collector of this pnp transistor is formed by the weakly p-doped semiconductor substrate 20. Finally, the emitter of this pnp transistor is formed by the strongly p-doped region 23. Both bipolar transistors likewise have parasitic base resistances, which are created by the weakly p-doped semiconductor substrate 20 on the one hand and the weakly n-doped well region 21 on the other hand.

In comparison with the lateral thyristor structure shown in Figure 2, the lateral thyristor structure shown in Figure 3 requires a much lower firing voltage for the thyristor, since the electric field between the strongly n-doped region 25 and the weakly p-doped semiconductor substrate 20 is much higher than the electric field between the weakly n-doped well region 21 and the weakly p-doped semiconductor substrate 20. Due to this feature, an avalanche breakdown between the strongly n-doped region 25 and the weakly p-doped semiconductor substrate 20 can be created much more easily than in the prior art of Figure 2.

The avalanche breakdown creates charge carriers between the strongly n-doped region 25 and the weakly p-doped semiconductor substrate 20. These charge carriers make the base of the npn transistor conducting, so that the npn transistor is turned on, and current begins to flow through the lateral thyristor structure, from the anode 27 to the cathode 26.

The firing voltage of the inventive lateral thyristor structure, shown in Figure 3, accordingly is essentially reduced to the "firing voltage" of the npn transistor, which is formed from the strongly n-doped region 25, the weakly p-doped semiconductor substrate, and the strongly n-doped region 22.

Another modification of the invention is to exchange the regions 23 and 24. This changes the characteristic of the pnp transistor 23, 21, 20, in that the effective

base width is increased; furthermore, 24 comes nearer to the electronic active zone, thus reducing the base bulk resistance. The thyristor thus can be caused to turn on with a delay and to turn off more easily. This exchange therefore is another possible way to optimize the system, but without any additional cost.

Compared to Figure 3, the embodiment of Figure 4 is a further development in the sense that, in place of an unsymmetric structure, a symmetric structure has been chosen, thus avoiding undesirable boundary effects. When the thyristors turn off, this avoids the situation whereby one of the component thyristors remains "hanging" alone. This would be a problem, since a single component thyristor requires only a small holding current. This is achieved especially in that the active regions of the thyristors are better decoupled from the boundary and adjoin one another more closely. If one starts from the structure of Figure 3, then this structure is mirrored for symmetrization, for example at the cathode. This results in two essentially identical, specularly inverted structures in the weakly p-doped semiconductor substrate 20. Consequently, the "duplicated" structure correspondingly likewise has a weakly n-doped well region 21', a strongly p-doped region 23', a strongly n-doped region 24', a strongly n-doped region 25', an anode 27', and field oxide regions 28', 29', and 30'. Furthermore, the structure is surrounded by a strongly p-doped substrate contact ring 31 ("boundary") with an anode terminal 26, so that, when firing during operation, the entire environment will not be brought into a latch-up state. Of course, more than two thyristors can also be combined, but an even number of them must be used for a symmetrical design of the structure.

The embodiment of Figure 5 is derived from the embodiment of Figure 3 in that a strongly n-doped region 41 is introduced into the field oxide region 29, so as to divide the field oxide region 29 into two component regions, with the strongly n-doped region 20 being situated in between. The equivalent circuit diagram of such a structure is shown in Figure 5a, and consists of a thyristor which has an anode 26, a cathode 27, and an internal connection 40 to a resistor 9. The internal connection 40 and also the resistor 9 are integrated into the thyristor 42 by diffusion and/or implantation.

In the circuit of Figure 1, an input signal (terminal 3) is present at the diode 7 and at the clamping circuit 6 (thyristor), and then passes through a metallic

connection to the interior circuit 4. The bond pad consequently is metallically connected to the interior circuit 4. However, this harbors risks, because the bond pad generally can reach large voltages before the protective structure becomes active, after a delay time. As an alternative in accordance with Figures 5 and 6, the signal path is displaced into the thyristor, resulting in a tolerable series resistor 9, which, starting from Figure 1, is connected between the corresponding connection line 8 of the interior circuit 4 and the input/output 3 (Figure 6). Thus the interior circuit 4 never directly "sees" the voltage at the input/output 3, but only the voltage at the thyristor. This greatly improves the protection of the interior circuit 4 in the case of ESD transients.

Figure 7 finally shows an embodiment of an inventive thyristor structure, which is especially suited for applications in which a large current flows through the connecting line 8 in Figure 6. This could result in undesirable turn-on and respectively in problems during turn-off. Compared to the embodiment of Figure 4, the terminal 40 in embodiment 7 is shifted so that the protective effect is indeed preserved, but the high currents on the connecting line 8 in Figure 6 do not flow in critical regions of the thyristor, that is not between the anode 26 and the cathode 27. Accordingly, with a view to Figure 3, the terminal 40, together with the strongly n-doped region 41, is introduced, for example, into the field oxide region 30 instead of the field oxide region 29 in the case of Figure 5.

Accordingly, the inventive lateral thyristor structures shown here very advantageously combine the high current-carrying capacity of a thyristor with the low "firing voltage" of a field oxide bipolar transistor.

Of course, in all the structures shown and discussed here, all n conductions can be exchanged with p conductions and vice versa, without impairing the function and principle of the present invention. All the doped regions 22, 23, 24 and 25, 31, 41, as well as the discussed well region 21, can be introduced into the semiconductor substrate 20 either by diffusion or by ion implantation. Combinations of diffusion and implantation are conceivable, which likewise do not impair the function or the principle of the present invention.